

Refine Search

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Terms	Documents
L1 same ((increas\$3 or decreas\$3) same (process\$3 near3 activity))	61

Database: <ul style="list-style-type: none"> US Pre-Grant Publication Full-Text Database US Patents Full-Text Database US OCR Full-Text Database EPO Abstracts Database JPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins
Search: <div style="border: 1px solid black; padding: 5px; width: 300px;"> <input style="width: 100%;" type="text" value="L3"/> </div> <div style="display: flex; justify-content: space-between; width: 100%;"> Refine Search Recall Text Clear Interrupt </div>

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

<u>L3</u>	L1 same ((increas\$3 or decreas\$3) same (process\$3 near3 activity))	61	<u>L3</u>
<u>L2</u>	L1 and ((increas\$3 or decreas\$3) same (process\$3 near3 activity))	116	<u>L2</u>
<u>L1</u>	monitor\$3 near10 (process\$3 near3 activity)	1227	<u>L1</u>

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result set

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L4 L3

0 L4

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 L1 same ((increas\$3 or decreas\$3) same (process\$3 near3 activity))

61 L3

L2 L1 and ((increas\$3 or decreas\$3) same (process\$3 near3 activity))

116 L2

L1 monitor\$3 near10 (process\$3 near3 activity)

1227 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(361/323 361/683 307/60 340/636 713/320 713/321 713/322 713/323 713/501 713/600 713/300).ccls.	7098

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L5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Refine Search
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side by side

Hit Count Set Name
result set

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L5 713/320-323,501,600,300;361/323,683;340/636;307/60.ccls.

7098 L5

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L4 L3

0 L4

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 L1 same ((increas\$3 or decreas\$3) same (process\$3 near3 activity))

61 L3

L2 L1 and ((increas\$3 or decreas\$3) same (process\$3 near3 activity))

116 L2

L1 monitor\$3 near10 (process\$3 near3 activity)

1227 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L3 and L5	9

Database:	US Pre-Grant Publication Full-Text Database
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<input type="text" value="L6"/> Refine Search	
Recall Text Clear Interrupt	

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Set Name **Query**
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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L6 L3 and L5

9 L6

L5 713/320-323,501,600,300;361/323,683;340/636;307/60.ccls.

7098 L5

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L4 L3

0 L4

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 L1 same ((increas\$3 or decreas\$3) same (process\$3 near3 activity))

61 L3

L2 L1 and ((increas\$3 or decreas\$3) same (process\$3 near3 activity))

116 L2

L1 monitor\$3 near10 (process\$3 near3 activity)

1227 L1

END OF SEARCH HISTORY

EAST - [Untitled1:1]

File View Edit Tools Window Help

Drafts Pending Active

L1: (201) monitor\$3 near10 ((processor near2 activity)
L2: (13) ll same ((increas\$3 or decreas\$3) same (processor

Search List Browse Open Clear

DBs USPAT Default operator: OR

Plurals Highlight all hit terms initially

BRS form I&R form Image Text HTML

Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error	Definition	Err
1	BRS	L1	201	monitor\$3 near10 (processor near2 activity)	USPAT	2004/11/03 15:24			
2	BRS	L2	13	ll same ((increas\$3 or decreas\$3) same (processor	USPAT	2004/11/03 15:25			

EAST - [Untitled1:1]

File View Edit Tools Window Help

New Workspace
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Active
L1: (201) monitor\$3 near10 (1)
L2: (13) ll same ((increas\$3
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash

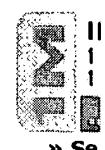
Search List Browse Delete Clear
DBs USPAT Default operator: OR Plurals Highlight all hit terms initially

ll same ((increas\$3 or decreas\$3) same (processor near2 activity))

BRS form AIS&R form Image Text HTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6681247 B1	20040120	22	Collaborator discovery method and system	709/217	707/10; 707/5;
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6636976 B1	20031021	13	Mechanism to control di/dt for a microprocessor	713/320	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6442652 B1	20020827	7	Load based cache control for satellite based CPUs	711/138	455/12.1; 711/154;
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6105053 A	20000815	39	Operating system for a non-uniform memory access	718/105	718/102
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5926053 A	19990720	30	Selectable clock generation mode	327/298	327/150; 327/159;
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5815693 A	19980929	30	Processor having a frequency modulated core clock based	713/501	713/601
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5815692 A	19980929	30	Distributed clock generator	713/501	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5809293 A	19980915	13	System and method for program execution tracing	712/227	712/233
9	<input type="checkbox"/>	<input type="checkbox"/>	US 5740410 A	19980414	25	Static clock generator	713/501	327/113
10	<input type="checkbox"/>	<input type="checkbox"/>	US 5632038 A	19970520	10	Secondary cache system for portable computer	713/324	711/144; 711/145
11	<input type="checkbox"/>	<input type="checkbox"/>	US 5506945 A	19960409	9	Use of "pipes" for the transfer of status	358/1.15	358/1.14; 358/1.16

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Results Key:

JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 Improving the data cache performance of multiprocessor operating systems

Chun Xia; Torrellas, J.;

High-Performance Computer Architecture, 1996. Proceedings. Second International Symposium on, 3-7 Feb. 1996

Pages:85 - 94

[\[Abstract\]](#) [\[PDF Full-Text \(1084 KB\)\]](#) **IEEE CNF**

2 Hardware evaluation of low power communication mechanisms for transport-triggered architectures

Pionteck, T.; Garcia, A.; Kabulepa, L.D.; Glesner, M.;

Rapid Systems Prototyping, 2003. Proceedings. 14th IEEE International Workshop on, 9-11 June 2003

Pages:141 - 147

[\[Abstract\]](#) [\[PDF Full-Text \(303 KB\)\]](#) **IEEE CNF**

3 Design verification of a super-scalar RISC processor

Turumella, B.; Kabakibo, A.; Bogadi, M.; Menon, K.; Thusoo, S.; Nguyen, L.; Saxena, N.; Chow, M.;

Fault-Tolerant Computing, 1995. FTCS-25. Digest of Papers., Twenty-Fifth International Symposium on, 27-30 June 1995

Pages:472 - 477

[\[Abstract\]](#) [\[PDF Full-Text \(468 KB\)\]](#) **IEEE CNF**



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Hardware evaluation of low power communication mechanisms for transport-triggered architectures

Pionteck, T. Garcia, A. Kabulepa, L.D. Glesner, M.

Inst. of Microelectron. Syst., Darmstadt Univ. of Technol., Germany

This paper appears in: **Rapid Systems Prototyping, 2003. Proceedings. 1 International Workshop on**

Publication Date: 9-11 June 2003

On page(s): 141 - 147

ISSN: 1074-6005

Number of Pages: xii+242

Inspec Accession Number: 7816888

Abstract:

The requirement for flexibility in IP-based designs **increases** the attractiveness of transport-triggered architectures as a suitable alternative to classic operation-**processors**. Since the performance of these architectures strongly depends on the communication mechanism, the optimization of the bus structure represents a design concern. In this work, a rapid prototyping methodology is employed in order to compare the power consumption and hardware requirements of several communication alternatives. Therefore, a generic test **processor** has been programmed onto an FPGA. By **monitoring** the switching **activity** and bus statistics under operation conditions, a fast and accurate evaluation of different bus coding schemes has been achieved.

Index Terms:

computer architecture field programmable gate arrays performance evaluation system design FPGA IP-based design architecture performance bus coding bus statistics bus structure optimization field programmable gate array flexibility requirement generic test processor prototype hardware evaluation hardware requirement low power communication mechanism operation-triggered processor power consumption processor design rapid prototyping methodology switching activity monitoring transport-triggered architecture

Documents that cite this document

There are no citing documents available in IEEE Xplore at this time.

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Search Results - Record(s) 1 through 9 of 9 returned.

1. Document ID: US 20030229816 A1

Using default format because multiple data bases are involved.

L6: Entry 1 of 9

File: PGPB

Dec 11, 2003

PGPUB-DOCUMENT-NUMBER: 20030229816

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030229816 A1

TITLE: Clock control arrangement for a computing system, power management system and processing unit including the same

PUBLICATION-DATE: December 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Meynard, Olivier	Vizille		FR	

US-CL-CURRENT: 713/600

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KOMC	Drawn Da
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2. Document ID: US 20030126478 A1

L6: Entry 2 of 9

File: PGPB

Jul 3, 2003

PGPUB-DOCUMENT-NUMBER: 20030126478

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030126478 A1

TITLE: Multiple mode power throttle mechanism

PUBLICATION-DATE: July 3, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Burns, James S.	Los Altos	CA	US	
Rusu, Stefan	Sunnyvale	CA	US	
Ayers, David J.	Fremont	CA	US	
Grochowski, Edward T.	San Jose	CA	US	
Eng, Marsha	Sunnyvale	CA	US	
Tiwari, Vivek	San Jose	CA	US	

US-CL-CURRENT: 713/300[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Drawn D](#) 3. Document ID: US 20020007463 A1

L6: Entry 3 of 9

File: PGPB

Jan 17, 2002

PGPUB-DOCUMENT-NUMBER: 20020007463

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020007463 A1

TITLE: Power on demand and workload management system and method

PUBLICATION-DATE: January 17, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Fung, Henry T.	San Jose	CA	US	

US-CL-CURRENT: 713/320[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Drawn D](#) 4. Document ID: US 6636976 B1

L6: Entry 4 of 9

File: USPT

Oct 21, 2003

US-PAT-NO: 6636976

DOCUMENT-IDENTIFIER: US 6636976 B1

TITLE: Mechanism to control di/dt for a microprocessor

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Drawn D](#) 5. Document ID: US 5926053 A

L6: Entry 5 of 9

File: USPT

Jul 20, 1999

US-PAT-NO: 5926053

DOCUMENT-IDENTIFIER: US 5926053 A

TITLE: Selectable clock generation mode

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequences](#) | [Attachments](#) | [Claims](#) | [KMC](#) | [Drawn D](#) 6. Document ID: US 5815693 A

L6: Entry 6 of 9

File: USPT

Sep 29, 1998

US-PAT-NO: 5815693
DOCUMENT-IDENTIFIER: US 5815693 A

TITLE: Processor having a frequency modulated core clock based on the criticality of program activity

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequencies](#) | [Attachments](#) | [Claims](#) | [KOMC](#) | [Draw. De](#)

7. Document ID: US 5815692 A

L6: Entry 7 of 9

File: USPT

Sep 29, 1998

US-PAT-NO: 5815692
DOCUMENT-IDENTIFIER: US 5815692 A

TITLE: Distributed clock generator

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequencies](#) | [Attachments](#) | [Claims](#) | [KOMC](#) | [Draw. De](#)

8. Document ID: US 5740410 A

L6: Entry 8 of 9

File: USPT

Apr 14, 1998

US-PAT-NO: 5740410
DOCUMENT-IDENTIFIER: US 5740410 A

TITLE: Static clock generator

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequencies](#) | [Attachments](#) | [Claims](#) | [KOMC](#) | [Draw. De](#)

9. Document ID: US 4670837 A

L6: Entry 9 of 9

File: USPT

Jun 2, 1987

US-PAT-NO: 4670837
DOCUMENT-IDENTIFIER: US 4670837 A
** See image for Certificate of Correction **

TITLE: Electrical system having variable-frequency clock

[Full](#) | [Title](#) | [Citation](#) | [Front](#) | [Review](#) | [Classification](#) | [Date](#) | [Reference](#) | [Sequencies](#) | [Attachments](#) | [Claims](#) | [KOMC](#) | [Draw. De](#)

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Terms	Documents
L3 and L5	9



US005926053A

United States Patent [19]

McDermott et al.

[11] Patent Number: 5,926,053

[45] Date of Patent: Jul. 20, 1999

[54] SELECTABLE CLOCK GENERATION MODE

[75] Inventors: Mark W. McDermott, Austin, Tex.;
Antoine L. Fourcroy, Fort Collins, Colo.

[73] Assignee: National Semiconductor Corporation,
Santa Clara, Calif.

[21] Appl. No.: 08/372,813

[22] Filed: Dec. 15, 1998

[51] Int. CL⁴ G06F 1/06

[52] U.S. Cl. 327/288; 327/291; 327/150;
327/159; 395/556; 395/558

[58] Field of Search 327/291, 298,
327/147, 149, 150, 153, 156, 158, 159,
161; 395/556, 558

[56] References Cited

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5,475,224	12/1995	Tomiya	327/59
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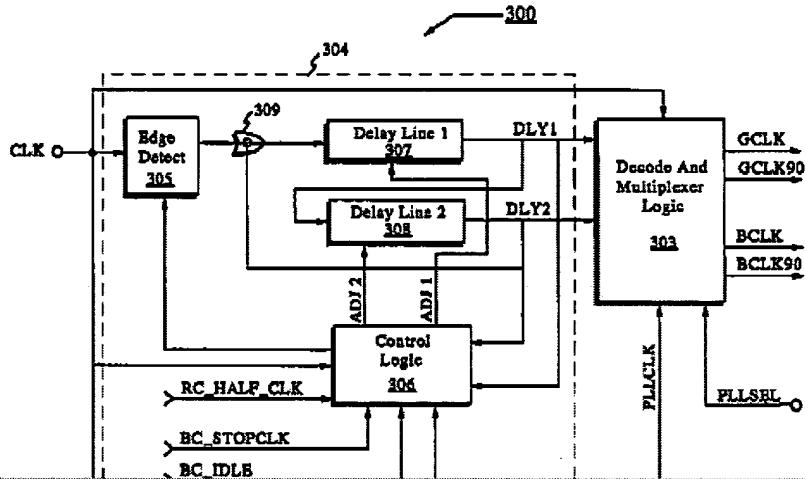
248836	2/1990	Japan	327/99
3238913	10/1991	Japan	327/99
5,268,020	10/1993	Japan	327/99

Primary Examiner—Tuan T. Lin
Attorney, Agent, or Firm—John L. Maxin

[57] ABSTRACT

A processing system includes circuitry and methodology for selecting clock generation modes between phase-locked loop and static delay line loop circuitries. The mode may be selectable through an externally accessible pin, an internal bond wire option, a boundary test scan control point, or other programmable register or control point.

14 Claims, 18 Drawing Sheets





United States Patent [19]

McDermott et al.

[11] Patent Number: 5,815,693

[45] Date of Patent: *Sep. 29, 1998

[54] PROCESSOR HAVING A FREQUENCY MODULATED CORE CLOCK BASED ON THE CRITICALITY OF PROGRAM ACTIVITY

[75] Inventor: Mark W. McDermott, Austin, Tex.; Antoine L. Fourcroy, Fort Collins, Colo.

[73] Assignee: National Semiconductor Corporation, Santa Clara, Calif.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No. 372,994

[22] Filed: Dec. 18, 1995

[51] Int. Cl. G06F 1/04; G06F 1/08

[52] U.S. Cl. 395/356; 395/550

[56] Field of Search 395/556, 559,

395/560, 750, 555, 750.04

[36] References Cited

U.S. PATENT DOCUMENTS

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5,473,767 12/1995 Kardach et al. 395/550
5,493,684 2/1996 Gephart et al. 395/750

FOREIGN PATENT DOCUMENTS

0 368 144 5/1990 Europees Pat. Off. G06F 1/32

Primary Examiner—Dennis M. Butler
Attorney, Agent, or Firm—John L. Maxin

[57] ABSTRACT

A processing system includes a clock synchronesh that receives indicia of critical activity from various functional units within the processing system and responsive to the indicia, ratchets down/up the frequency of a clock output signal to at least one of the functional units to reduce power consumption. The determination of critical activity is preferably made according to a heuristic internal to a processor under software or hardware control.

9 Claims, 18 Drawing Sheets

